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Continuation of Box II.2

Claims Nos.: 1-6

Claims 1 and 6 comprise an electronic circuit arrangement comprising two components - a clock fail circuit generating an error signal upon the absence of an external clock signal and an asynchronous processor arranged for receiving said error signal.

Synchronous processors need a clock signal. Since synchronous processors stop functioning as soon as the clock signal stops, they cannot themselves check whether the clock signal is arriving correctly. Thus, in addition to the clock signal, synchronous processors need a clock fail circuit.

The whole point of an asynchronous processor is that it does not require a clock signal. And since the asynchronous processor does not require any clock, it does not need a clock fail circuit either, because it does not care if any clock fails.

At the end of claims 1 and 6 it is claimed that in response to the receipt of the error signal the asynchronous processor "brings the electronic circuit arrangement into a pre-defined state". This passage is extremely vague - some passages in the description suggest that it may refer to a state triggered by a reset or interrupt signal. Moreover, the passage does not make technical sense. The asynchronous processor is not affected by the clock failure, it works fine, so why should it be interrupted? The clock fail circuit also works fine, after all it has correctly detected that clock failure, so why should it be reset? And if it is reset before the clock failure was repaired, it will immediately detect another clock failure and issue another reset/interrupt signal. The only thing which has failed and which would require resetting is the clock signal generator, but that is not part of the circuit arrangement in the claims, and it is not reset.

In other words, when a component outside the circuit fails, only the components inside the circuit, which have not failed, are reset. This configuration does not appear to make sense from a technical point of view, and consequently it would be impossible to find such a configuration in a search.

There is one embodiment of the invention in which an integrated circuit comprising the arrangement of claims 1 and 6 is described (see pages 4-5 and Figure 4). In this configuration, the IC additionally contains the clock generator and at least one synchronous circuit block. In such a configuration the combination of the asynchronous processor and the clock fail circuit does make sense. While a clock failure still would not directly affect the asynchronous processor, it would affect the synchronous circuit. Now the clock fail circuit is needed, and now it makes sense to send an interrupt to the asynchronous circuit - not to bring it into a predetermined state, but to let it perform a software routine handling the condition of a failing clock circuit. This makes technical sense, it is free of intrinsic contradictions, and the search

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was directed to this embodiment.

The applicant's attention is drawn to the fact that claims relating to inventions in respect of which no international search report has been established need not be the subject of an international preliminary examination (Rule 66.1(e) PCT). The applicant is advised that the EPO policy when acting as an International Preliminary Examining Authority is normally not to carry out a preliminary examination on matter which has not been searched. This is the case irrespective of whether or not the claims are amended following receipt of the search report or during any Chapter II procedure. If the application proceeds into the regional phase before the EPO, the applicant is reminded that a search may be carried out during examination before the EPO (see EPO Guideline C-VI, 8.5), should the problems which led to the Article 17(2) declaration be overcome.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
I/IB2005/050575

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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